- 6. (a) What is an ASM chart? Briefly discuss components of ASM chart.
 - (b) Draw the ASM chart for sequence detector to detect the sequences 1011 and 1101. It generates output 1 when sequence is detected. Overlapping is not permitted. 8

Unit IV

- 7. (a) Explain working of a two-input TTL NAND gate with the help of circuit diagram. 7
 - (b) Explain working of 2-input CMOS NAND gate. What is the advantage of active load?
- 8. (a) Explain need of using PLDs in digital system design.
 - (b) Compare CPLD and FPGA.
 - (c) Design and implement full adder circuit using PLA.

No. of Printed Pages : 5

Roll No.

18C3

B.Tech. EXAMINATION, 2024

(3rd Semester)

(C Scheme) (Main & Re-appear)

(CSE, ECE)

ECE203C

DIGITAL SYSTEM DESIGN

Time: 3 Hours] [Maximum Marks: 100

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note: Attempt *Five* questions in all, selecting *one* question from each Unit. Q. No. 9 is compulsory. All questions carry equal marks.

(4-D24-02/24) M-18C3

P.T.O.

Unit I

1. (a) Simplify following expression using
Boolean algebra: 4

$$F = (\overline{A} + B)(A + B + D)\overline{D}$$

(b) Realize XOR function using NAND logic.

4

(c) Minimize the following expression using K-map and realize using NOR Gates: 7

 $F = \Pi M(1, 2, 3, 8, 9, 10, 11, 14)*d(7,15)$

2. (a) Reduce the following expression using 3-variable Map: 7

$$F = \overline{A} + \overline{B} + \overline{C} + \overline{A}BC + \overline{A}BCF$$

 $+ \overline{A}B\overline{C} + A\overline{B}CD + AB\overline{C}\overline{F}$

(b) Design and implement 4-bit Gray to Binary code converter using suitable logic gates.

2

8

Unit II

- 3. (a) Implement a full subtractor using two4: 1 multiplexers.
 - (b) Design a BCD adder using 4-bit binary adder. 8
- 4. (a) Draw the circuit diagram for J-K flip flop using NAND Gates. Give its truth table and explain race around condition.
 - (b) Discuss applications of shift registers. 8

Unit III

- 5. (a) Design a 3-bit odd parity generator usingJ-K flip flops.
 - (b) Design a sequence detector to detect the non-overlapping sequences 1011 and 1101.It generates output 1 when sequence is detected.

3

(4-D24-02/25) M-18C3

P.T.O.

Compulsory Question:

- 9. Explain the following terms: 15
 - (a) Canonical forms
 - (b) Parallel adder
 - (c) Edge-triggered FF
 - (d) Serial binary adder
 - (e) Interfacing of different logic families

Compulsory Question:

- 9. Explain the following terms:
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15